JC05 Rec'd PCT/PTO 17 JUN 2005

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			
INFORMATION DISCLOSURE STATEMENT		Docket Number: 10191/4188 10/539495	
Application Number To Be Assigned	Filing Date Herewith	Examiner	Art Unit
Invention Title **DEVICE AND METHOD FOR FORMING A SIGNATURE**		Werner HARTER et al.	

Address to:

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

I. In accordance with the duty of disclosure under 37 C.F.R. § 1.56 and in conformance with the procedures of 37 C.F.R. §§ 1.97 and 1.98 and M.P.E.P. § 609, attorney for Applicants hereby brings the following references to the attention of the Examiner. These references are listed on the attached modified PTO Form No. 1449. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

II. A copy of each patent, publication or other information listed on the modified PTO form 1449 is enclosed, except as otherwise indicated on the modified PTO form 1449

Dated: 6/17/05

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT PTO FORM 1449	Atty. Docket No. 10191/4188	Serial No. To Be Assigned 10/539495
	Applicant(s) HARTER et al.	
	Filing Date Herewith	Group To Be Assigned

U. S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NUMBER	PATENT DATE	NAME	CLASS	SUBCLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS

EXAMINER'S INITIALS		AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
		Built-In Test for VLSI: Pseudorandom Techniques by Paul H. Bardell, William H. McAnney and Jacob Savir; pp. 124 et seq.*
		A Linear Code-Preserving Signature Analyzer COPMISR; Hlawiczka et al; VLSI Test Symposium, 1997 – 15th IEEE Monterey, CA USA 27 April – 1 May 1997.; pp. 350-355.**
		Low Cost BIST for EDAC Circuits; Badura et al; Test Symposium, 1997 (ATS '97), Proceedings, Sixth Asian Akita, Japan 17-19 November 1997; pp. 410-415.**
		Utilization of On-Line (Concurrent) Checkers During Built-In-Self-Test and Vice Versa; Gupta et al.; IEEE Transactions on Computers; 1 January 1996; pp. 63-73.**
		Design of t-UED/AUED Codes from Berger's AUED Code; Biswas et al.; VLSI Design, 1997, Proceedings, Tenth International Conference on Hyderabad; 4-7 January 1997; pp. 364-369.**
EXAMINER		DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

*Described in specification.

**Copy of reference is not enclosed because reference is cited in Search Report (copy of reference provided by International Searching Authority).